PATENT CLAIMS

1. An insulated gate bipolar transistor, comprising

- a semiconductor substrate (2) having a top and a bottom surface, a gate insulation film (41) formed on the top surface, said gate insulation film (41) comprising at least one contact opening,
- said semiconductor substrate (2) comprising
  - an emitter layer (21) of first conductivity type adjoining said bottom surface,
  - a drift region (22) of second conductivity type adjoining said emitter layer (21),
  - a channel region (7) of first conductivity type formed in the drift region (22) underneath the contact opening and underneath part of the gate insulation film (41),
  - one or more source regions (6) of second conductivity type disposed in the channel region (7) and delimiting a base contact area (821);
- a gate electrode (5) formed on the gate insulation film (41),
- a bottom metallization layer (1) formed on the bottom surface,
- a top metallization layer (9) covering the contact opening,

characterized in that

- a first base region (81) of first conductivity type is disposed in the channel region (7) so that it encompasses the one or more source regions (6), but does not adjoin

the second main surface underneath the gate oxide layer (41), and in that

- a second base region (82) of first conductivity type is disposed in the semiconductor substrate (2) underneath the base contact area (821) so that it partially overlaps with the channel region (7) and with the first base region (81).

2. The insulated gate bipolar transistor as claimed in claim 1, wherein a depth d_{B2} of the second base region (82) exceeds a depth d_C of the channel region (7) by at least a factor of 1.5, i.e. $d_{B2} > 1.5\ d_C$.

3. The insulated gate bipolar transistor as claimed in claim 1 or 2, characterized in that a doping p_{B1} concentration of the first base region (81) and a doping concentration p_{B2} of the second base region (82) are at least 5 times higher than a doping concentration p_C of the channel region (7), i.e. $p_{B1} > 5.0\ p_C$, $p_{B2} > 5.0\ p_C$.

4. The insulated gate bipolar transistor as claimed in one of the previous claims, characterized in that at least one protection region (221) of second doping type is disposed in the drift region underneath the gate oxide layer (41), said protection region (3) adjoining both the channel region (7) and the bottom surface of the semiconductor substrate (2).

5. The insulated gate bipolar transistor as claimed in one of the previous claims, characterized in that a thickness of the gate insulation film (41, 43) increases at a distance l from the contact opening.

AMENDED CLAIMS
[received by the International Bureau on 16 March 2005 (16.03.2005);
original claim 1 amended; remaining claims unchanged (1 page)]

1. An insulated gate bipolar transistor, comprising

- a semiconductor substrate (2) having a top and a bottom surface, a gate insulation film (41) formed on the top surface, said gate insulation film (41) comprising at least one contact opening,
- said semiconductor substrate (2) comprising
  - an emitter layer (21) of first conductivity type adjoining said bottom surface,
  - a drift region (22) of second conductivity type adjoining said emitter layer (21),
  - a channel region (7) of first conductivity type formed in the drift region (22) underneath the contact opening and underneath part of the gate insulation film (41),
  - one or more source regions (6) of second conductivity type disposed in the channel region (7) and delimiting a base contact area (821);
- a gate electrode (5) formed on the gate insulation film (41),
- a bottom metallization layer (1) formed on the bottom surface,
- a top metallization layer (9) covering the contact opening and being contacted by one or more source regions (6),

characterized in that

- a first base region (81) of first conductivity type is disposed in the channel region (7) so that it encompasses the one or more source regions (6), but does not adjoin the second main surface underneath the gate oxide layer (41), and in that
- a second base region (82) of first conductivity type is confined in the semiconductor substrate (2) to a region underneath the base contact area (821) so that it partially overlaps with the channel region (7) and with the first base region (81).